Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KENNETH D. CHAPMAN
and
STEVEN P. YOUNG

Appeal No. 2000-1204
Application No. 08/786,818

HEARD: FEBRUARY 21, 2002

Before HAIRSTON, RUGGIERO, and SAADAT, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1, 3, 4 and 7 through 10.

The disclosed invention relates to the use of a dedicated AND gate in a configurable logic block (CLB). The CLB is used in a field programmable gate array.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

> 1. A configurable logic block (CLB) for use in a field programmable gate array, the CLB comprising:
>
> a plurality of input lines;
>
> a carry-in line;
>
> a carry-out line;
>
> at least one lookup table, each such lookup table receiving input signals from N of the plurality of input lines and having an output line;
>
> a dedicated AND gate receiving two input signals from two of the plurality of input lines; and
>
> a carry chain having a carry input coupled to the carry-in line and a carry output coupled to the carry-out line, and at least one carry multiplexer controlled by the lookup table output line, each such multiplexer having at least two inputs, one such input being provided by the carry-in line, and the other such input being provided by the AND gate.

The references relied on by the examiner are:

New et al. (New)	5,481,206	Jan. 2, 1996
Rose et al. (Rose)	5,724,276	Mar. 3, 1998 (filed Jun. 17, 1996)

Claims 1 and 3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rose.

Claims 4 and 7 through 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rose in view of New.

Reference is made to the briefs (paper numbers 15 and 17) and the answer (paper number 16) for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 1, 3, 4 and 7 through 10.

The examiner's rejection is as follows:

> As per claim 1, Rose et al[.] discloses in Fig. 4a a configurable logic block (CLB) for use in a field programmable gate array (FPGA). The CLB clearly has a plurality of input lines, a carry-in line, a carry-out line, at least one lookup table (LUT F), and a carry chain having a carry input coupled to the carry-in line and a carry output coupled to the carry-out line. The carry chain also has at least one carry multiplexer (CMUX) controlled by the output of the lookup table and having one input being provided with the carry- in line and another input being provided with an AND logic of 2 input lines (a0b1) which are also the input lines to the lookup table. It [is] noted that Rose et al. discloses the AND logic being provided by another lookup table (LUT G), whereas, in the present invention the AND logic [is] being provided by a dedicated AND gate. However, in the field of FPGA, the use of a lookup table and the use of a gate to provide a logic function are both well known and are art recognized equivalents with a trade off between

the complexity and the flexibility of a CLB. Further, since Rose et al. clearly disclose in Fig. 4a that an output of the CMUX is provided with an AND logic of 2 input lines (a0b1) of the LUT F, a person of ordinary skill in the art

> would have found it obvious to provide Rose et al. with an AND gate in place of the LUT G for providing the AND logic to the CMUX in order to reduce the circuitry in the CLB. [Answer, pages 3-4.]

Appellants argue inter alia (brief, pages 4 and 5) that "the Office Action has not provided any support for its assertion that 'the use of a LUT and the use of a logical gate for providing a logical function are art recognized equivalents,'" and that "it is insufficient to assert that one of ordinary skill in the art might have been motivated to replace LUT G with a random single gate."

In In re Zurko, 258 F.3d, 1379, 1386, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001), the Court stated that:

> With respect to core factual findings in a determination of patentability . . . the . . . [Office] cannot simply reach conclusions based on its own understanding or experience - or on its assessment of what would be basic knowledge or common sense. Rather, the . . . [Office] must point to some concrete evidence in the record in support of these findings.

In view of the complete absence of any evidence in the record to support the examiner's finding that "the use of a lookup table and the use of a gate to provide a logic function are both well known and are art recognized equivalents," we cannot agree with the examiner that the skilled artisan would have

found it obvious "to provide Rose et al. with an AND gate in place of the LUT G for providing the AND logic to the CMUX." To the contrary, it appears that the LUT G performs an arithmetic multiplication function, as opposed to a logical ANDing function, when it "performs the calculation a**0**b**1**" (column 3, lines 23 and 24; Figure 4a). In the absence of such evidence, the examiner has not presented a prima facie case of obviousness of the claimed subject matter. Thus, the obviousness rejection of claims
1 and 3 is reversed. The obviousness rejection of claims 4 and
7 through 10 is likewise reversed because the multiplexer teachings of New do not cure the noted shortcomings in the teachings of Rose and the examiner's finding of obviousness.

DECISION

The decision of the examiner rejecting claims 1, 3, 4 and 7 through 10 under 35 U.S.C. § 103(a) is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
JOSEPH F. RUGGIERO Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
MAHSHID D. SAADAT Administrative Patent Judge	)	

KWH:hh

EDEL M. YOUNG
XILINX, INC.
2100 LOGIC DR.
SAN JOSE, CA 95124